UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/816,926	03/23/2001	Ralf Arnold	GR 98 P 8107 P	6101

24131 7590 05/02/2005

LERNER AND GREENBERG, PA
P O BOX 2480
HOLLYWOOD, FL 33022-2480

EXAMINER	
COLEMAN, ERIC	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 05/02/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/816,926	ARNOLD ET AL.	
	Examiner	Art Unit	
	Eric Coleman	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 April 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Applicant's request for reconsideration final of the rejection is persuasive. However, after further search and consideration the Examiner is withdrawing the finality last office action and reopening prosecution in order to apply a new ground of rejection.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-5,16-23,25 are rejected under 35 U.S.C. 102(b) as being anticipated by Wilkinson (patent No. 5,870,619).

4. Wilkinson taught the invention as claimed including a data processing ("DP") system (e.g., see figs. 4, 5,7,8,12,18,20) comprising: configurable hardware block (e.g., see col. 17, lines 3-18) comprising a universal configurable unit being selectively configured to read data stored in a memory unit (e.g., see col. 23, lines 45-63), to process the data in at least one arithmetic and logical processing units(e.g., see col. 23 lines 45-63), and to write data representing a result of the processing to the memory unit (e.g., see col. 24, lines 5-13 and fig. 7), the universal configurable unit having an asynchronous combinational circuit (e.g., see fig.7) to asynchronously link components of the universal configurable unit (e.g., see col. 69, line 26-col. 70, line 38, and 72,lines

35-46) and the universal configurable unit being capable of interacting autonomously with external hardware (e.g., see col. 25, lines 30-55 and 72, lines 6-33).

5. As to the capability of autonomously interacting with external hardware (claim 1) the Wilkinson universal configurable unit at least is capable of interacting autonomously with external hardware comprising other universal configurable units (PMEs) (e.g., see col. 69, line 26-col. 70, line 38). As to this limitation, although met by the Wilkinson reference, the limitation uses the "capable of" terminology that does not positively claim the limitation. Therefore this limitation is given no weight.

6. As per claim 2, Wilkinson taught the hardware block is configured for interaction with external hardware comprising instructing the memory unit to accept data supplied by the external hardware in response to specific event (interrupts) (e.g., see col. 24, lines 5-13).

7. As per claim 3, Wilkinson taught the configurable hardware block was configured for interaction with external hardware comprising outputting one of data and signal to the external hardware (e.g., see col. 32, line 65-col. 33, line 25).

8. As per claim 4, Wilkinson taught external hardware was selected from the group consisting of other configurable hardware blocks, a control unit operating in parallel or at a supervisory level, and other components of a system containing the configurable hardware block (e.g., see col. 37, lines 1-56).

9. As per claim 5, Wilkinson taught the data and/or signals output to the external hardware are used to signal specific states or events (e.g., see col. 45, lines 48-63).

10. As per claim 16,17 Wilkinson taught a plurality of configurable units selected from the group consisting of subunits selectively configurable to a required function, configurable data paths, and configurable signal paths (e.g., see col. 21, line 3-col. 22, line 36) wherein paths to the external hardware exist or can be established. As to the "can be established limitation even though Wilkinson taught the limitation this limitation is not positively claimed and therefore is given no weight.

11. As per claim 18, Wilkinson taught the hardware block comprising memory with general-purpose registers (e.g., see col. 23, lines 23-39).

12. As per claim 19, Wilkinson taught hardware block configurable on a basis of instructions of instruction sequences, and configurable to execute operations or operation specified by the instructions or instruction sequences (e.g., see col. 13, line 1-col. 14,line 16 and col. 49, line 49-col. 50, line 9). Further as per claim 20, the configurable blocks in the Wilkinson system meet the hyperblock dimension limitation to the extent claimed (e.g., see col. 23, lines 12-63 and col. 13, lines 14-44 and col. 34, lines 19-col. 36, line 30). As per claim 21,22,23 Wilkinson taught the hardware block was used to replace a specific circuit or circuits, and configured to test the hardware block(e.g., see col. 21, lines 34-57).

13. As per claim 25, Wilkinson taught a memory in the hardware block for storing interim results (e.g., see fig. 7).

Claim Rejections - 35 USC § 103

14. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

15. Claims 6-15,24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wilkinson (patent No. 5,870,619).

16. Wilkinson taught the invention substantially as claimed including a data processing ("DP") system (e.g., see figs. 4, 5,7,8,12,18,20) comprising: configurable hardware block (e.g., see col. 17, lines 3-18) comprising a universal configurable unit being selectively configured to read data stored in a memory unit (e.g., see col. 23, lines 45-63), to process the data in at least one arithmetic and logical processing units(e.g., see col. 23 lines 45-63), and to write data representing a result of the processing to the memory unit (e.g., see col. 24, lines 5-13 and fig. 7), the universal configurable unit having an asynchronous combinational circuit (e.g., see fig.7) to asynchronously link components of the universal configurable unit (e.g., see col. 69, line 26-col. 70, line 38, and 72,lines 35-46) and the universal configurable unit being capable of interacting autonomously with external hardware (e.g., see col. 25, lines 30-55 and 72, lines 6-33).

17. As to the capability of autonomously interacting with external hardware (claim 1) the Wilkinson universal configurable unit at least is capable of interacting autonomously with external hardware comprising other universal configurable units (PMEs) (e.g., see col. 69, line 26-col. 70, line 38). As to this limitation, although met by the Wilkinson

reference, the limitation uses the "capable of" terminology that does not positively claim the limitation. Therefore this limitation is given no weight.

18. As per claim 2, Wilkinson taught the hardware block is configured for interaction with external hardware comprising instructing the memory unit to accept data supplied by the external hardware in response to specific event (interrupts) (e.g., see col. 24, lines 5-13).

19. As per claim 3, Wilkinson taught the configurable hardware block was configured for interaction with external hardware comprising outputting one of data and signal to the external hardware (e.g., see col. 32, line 65-col. 33, line 25).

20. As per claim 4, Wilkinson taught external hardware was selected from the group consisting of other configurable hardware blocks, a control unit operating in parallel or at a supervisory level, and other components of a system containing the configurable hardware block (e.g., see col. 37, lines 1-56).

21. As per claim 5, Wilkinson taught the data and/or signals output to the external hardware are used to signal specific states or events (e.g., see col. 45, lines 48-63).

22. As per claim 6,7 Wilkinson did not expressly detail a timer generation unit generating a clock signal for the memory unit. Wilkinson, however, taught a cluster synchronizer for synchronizing the operation of the clusters of hardware blocks (e.g., see col. 45, lines 8-22) and a cluster controller that interfaces the hardware blocks and operates synchronously in SIMD mode (e.g., see col.45, lines 24-38). Therefore one of ordinary skill would have been motivated to provide a timer generation unit to generate a clock signal for synchronizing the transfer of data and/or instructions to from the

memory of each hardware block. This would have comprises signals from a hardware block and an external hardware block for accomplishing the synchronization.

23. As per claims 8-11, Wilkinson taught an operation of sequence of operations to be executed repeatedly (looping of the operations of acquiring messages from neighbor nodes) in the hardware block had been executed a specified number of times (e.g., see col. 39, lines 22-37). Wilkinson also taught sequencing of tasks and use of interrupts to manage the network in transfer of data (e.g., see col. 39, lines 38-61). Therefore one of ordinary skill in the DP art would have been motivated to use the interrupts to report the completion of a sequence of operations to manage the transfers of data via the network.

24. As per claim 12, Wilkinson since Wilkinson taught looping of processes and routing data/from specified hardware blocks (e.g., see col. 39, lines 21-61). Therefore one of ordinary skill would have been motivated to use a comparison unit to generate the interrupt report at least to ensure that the data was sent to the proper destination and/or the data was sent after the predetermined process had completed. Further (claim 13) since Wilkinson taught plural interrupts and processes then one of ordinary skill would have been motivated to selected from comparison of conditions or signals to provide the proper interrupt and checking whether the conditions for issuing the interrupt were true of false at least to issue or mask the interrupt.

25. As to claim 14,15 Wilkinson taught floating point operations. The group of arithmetic compare operations were well known in the DP art to comprise greater than, greater than or equal to, not equal to, smaller than, and smaller than or equal to. Also since Wilkinson taught looping of processes theses conditions were well known for use

in looping instructions to determine if a loop is complete (e.g., see col. 39, lines 21-61). Consequently one of ordinary skill in implementing the Wilkinson system would have been motivated select from these comparisons to determine when the loops were complete. Further a well known means for comparison of signal comprised series connections of multiplexers and consequently one of ordinary skill would have been motivated to use series connected multiplexers to implement the comparison function.

26. As per claims 24, The Wilkinson system is a scalable configurable system for multiple dimensions that operates in multiple SIMD and MIMD modes for massively parallel processing of data. Therefore one of ordinary skill would have been motivated to use the Wilkinson system for applications that required these criteria. Identification and cryptography comprises these criteria and therefore one of ordinary skill would have been motivated to use the Willkinson system to process identification and cryptography applications.

27. Applicant's arguments with respect to claims 1-25 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Martin (patent No. 6,658,550) disclosed a pipelined asynchronous processor (e.g., see abstract).

Martin (patent No. 6,152,613) disclosed a circuit implementation for asynchronous processors (e.g., see abstract).

Siemers (patent No. 6,061,367) disclosed a processor with pipelining structure and method for high speed calculation (e.g., see abstract and figs. 2,3).

Molvig (patent No. 5,377,129) disclosed a massively parallel data processor having combnational logic (e.g., see abstract).

Caulk (patent No. 5,603,047) disclosed a superscalar microprocessor that mutiplexes data between internal elements (e.g., see abstract and figs. 4,5,17).

Thomann (patent No. 5,748,635) disclosed a multiport interface comprising combinational logic coupling asynchronous devices (e.g. see abstract and fig.2).

Butts (patent No. 5,796,623) disclosed a system for performing computations with electrically reconfigurable logic devices (e.g., see abstract).

Potash (patent No. 4,760,518) disclosed a bi-directional system for supporting superposition of vector and scalar operations in a computer (e.g., see abstract).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric Coleman whose telephone number is (571) 272-4163. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

EC

ERIC COLEMAN
PRIMARY EXAMINER